REMARKS

Claim Rejections - 35 U.S.C. § 102 and 103

The Examiner has rejected claims 1 and 20 under 35 USC 102(b) as unpatentable over Lee et al. (U.S. Patent No. 6,850,683). The Examiner has rejected claims 4-5 under 35 USC 103(a) as unpatentable over Lee et al. (U.S. Patent No. 6,850,683) in view of Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press (1986)). The Examiner has rejected claims 3 and 22 under 35 USC 103(a) as unpatentable over Ishida et al. (U.S. Patent No. 4,695,122). The Examiner has rejected claims 6, 9, and 10 under 35 USC 103(a) as unpatentable over Lee et al. (U.S. Patent No. 6,850,683) in view of Hembree et al. (U.S. Patent No. 6,224,713). The Examiner has rejected claim 7 under 35 USC 103(a) as unpatentable over Lee, et al. (U.S. Patent No. 6,850,683) in view of Hembree et al. (U.S. Patent No. 6,224,713) and further in view of Li (U.S. Patent No. 5,976,767). The Examiner has rejected claim 8 under 35 USC 103(a) as unpatentable over Lee, et al. (U.S. Patent No. 6,850,683) in view of Hembree et al. (U.S. Patent No. 6,224,713) and further in view of Li (U.S. Patent No. 5,976,767) in further view of Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press (1986)). The Examiner has rejected claims 11 and 12 under 35 USC 103(a) as unpatentable over Lee, et al. (U.S. Patent No. 6,850,683) in view of Hembree et al. (U.S. Patent No. 6,224,713), in further view of Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press (1986)). The Examiner has rejected claim 2 under 35 USC 103(a) as unpatentable over Patel, et al. (U.S. Patent No. 2004/0240822) in view of Newn et al. (U.S. Patent No. 3,999,835). The Examiner has rejected claim 13 under 35 USC 103(a) as unpatentable over Patel, et al. (U.S. Patent No. 2004/0240822), in further view of Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press (1986)), in view of Li et al. (U.S. Patent No. 5,976,767) and

further in view of Ilardi (U.S. Patent No. 5,466,689). The Examiner has rejected claims 16 and 21 under 35 USC 103(a) as unpatentable over Lee, et al. (U.S. Patent No. 6,850,683).

The Applicant respectfully traverses. The cited references, either individually or in combination, fail to teach or render obvious all of the elements of the claimed invention. In particular, the cited references fail to teach the element of independent claims 1 and 20 of "etching a waveguide isotropically." Lee describes etching a waveguide core in Col. 2 lines 59 – 61: "...a waveguide core 108 after a typical patterning process including photolithography and etching of the layer 102." Lee fails to disclose that the etching of the layer 102 to the form the waveguide core 108 is isotropic. Patel also fails to teach etching a waveguide isotropically and instead teaches etching a sacrificial polysilicon layer 60 that is formed over a polysilicon waveguiding structure with a plasma-based etching technique in order to form rounded top edges in the underlying polysilicon waveguiding structure 54 by transferring the rounded features of the sacrificial polysilicon layer 60 to the structure 54 (see paragraph 39). The remaining references, Wolf, Ishida, Hembree, and Newn also fail to teach etching a waveguide isotropically. Therefore, the Applicant respectfully submits that the independent claim 1 and 20, and the claims that depend upon and incorporate the limitations of the independent claims 1 and 20, are not obvious in view of the cited references.

The Examiner has rejected claim 17-18 under 35 USC 103(a) as unpatentable over Patel, et al. (U.S. Patent No. 2004/0240822), in further view of Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press (1986)), in view of Li et al. (U.S. Patent No. 5,976,767). The Examiner has rejected claim 19 under 35 USC 103(a) as unpatentable over Patel, et al. (U.S. Patent No. 2004/0240822), in further view of Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press (1986)), in view of Li et al. (U.S. Patent No. 5,976,767) and further in view of Liu et al. (U.S. Patent No. 4,817,652). The Applicant respectfully traverses. The cited references, either individually or in combination, fail to teach or render obvious all of the elements of independent claim 17, in particular the elements of "*etching the amorphous silicon layer with an anisotropic dry plasma etch to form at least one waveguide; [and] submerging the at least one waveguide in an ammonia*

hydroxide isotropic wet etch solution". In contrast, Patel teaches etching a sacrifical polysilicon layer 60 that is formed over a polysilicon waveguiding structure with a plasma-based etching technique in order to form rounded top edges in the underlying polysilicon waveguiding structure 54 by transferring the rounded features of the sacrificial polysilicon layer 60 to the structure 54 (see paragraph 39). Wolf, Li, and Liu also fail to teach these elements. Therefore, the Applicant respectfully submits that the independent claim 17, and the claims that depend upon and incorporate the limitations of claim 17, are not obvious in view of the cited references.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: December 19, 2005

HMolleur 12/19/05

Heather M. Molleur
Reg. No. 50,432

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300